## REMARKS

The application includes claims 1-16 prior to entering this amendment.

The examiner rejects claims 1-7 and 13-16 under 35 U.S.C. § 102(b) as being anticipated by Lee et al. (U.S. Patent 5,355,415).

The examiner rejects claims 8-12 under 35 U.S.C. § 103(a) as being unpatentable over Lee in view of Amrany (U.S. Patent 5,530,959).

The applicants amend claims 1-4 and 6-16, adds claims 17-20, and cancels claim 5 without prejudice.

The application remains with claims 1-4 and 6-20 after entering this amendment.

The applicants add no new matter and request reconsideration.

### Claim Rejections Under §§ 102 and 103

The examiner rejects claims 1-7 and 13-16 as old over Lee. The applicants traverse the rejections for the reasons that follow.

Lee discloses a parallel distributed sample scrambling and descrambling system. In Lee's system, a parallel shift register generator generates parallel sequences for parallel scrambling using a plurality of shift registers and a plurality of module-2 adders.[1] Lee's system further includes a sampling means for generating samples from the parallel shift register generator depending on available transmission channel slots and a parallel scrambling means for performing parallel scrambling by module-2 adding the parallel sequences from the parallel shift register generator to the parallel input data.[2]

Claim 1 recites *digital logic means for determining a subset of a serial sequence of scramble bits by applying a generating polynomial to the serial sequence of scramble bits* and *generating means for generating the subset responsive to an immediately preceding state of the subset.* Claim 8 recites *digital logic means for determining a subset of the serial sequence of scrambler bits, the subset being determined based on an immediately preceding subset of the serial sequence of scrambler bits.* Claim 13 recites *b) determining a subset of the recurring serial sequence of scrambler bits based on an immediately preceding subset of the recurring serial*

[1] Abstract.
[2] Id.

*sequence of scrambler bits* and *c) generating the subset where, for each bit of the plurality of data bits, at least one bit of the appropriate subset is associated therewith.* Claim 17 recites *a register block to store a current state of a subset of a recurring serial sequence of scramble bits* and *a predict logic block to generate the subset responsive an immediately preceding state of the subset.*

The examiner points to Lee's figures 4, 5, 6A (blocks 61, 71, and 72), 8B, and column 6, lines 17-20, and column 10, lines 6-51 to reject the prior incarnation of the digital logic means and the generating means recited in claim 1. While Lee's parallel shift register generator (PSRG) 61 "includes a shift register generator engine 71 for generating a state transition matrix for shift registers and a parallel sequence generating circuit 72 for generating parallel sequences,"[3] it does not determine a subset of a serial sequence of scramble bits much less determine a subset of a serial sequence of scramble bits by applying a generating polynomial as recited. Lee discloses generating a parallel sequence at the output of generating block 72 but it does not appear to disclose that it generates that parallel sequence using a *subset of a serial sequence* of scramble bits as is required by the claim. And although Lee does mention a state transition matrix Tp, it does not disclose sufficient detail for the examiner to conclude that it discloses *generating the subset responsive to an immediately preceding state of the subset.* Although Lee discloses that the "state transition matrix Tp...can be obtained from the paper by D. W. Choi, entitled 'Parallel scrambling techniques for digital multiplexer' AT&T Tech. J, pp. 123-136, Sept/Oct. 1986,"[4] Lee does not incorporate Choi by reference nor has the examiner cited Choi against the present application. Under these circumstances, the applicants contend that the examiner must provide a proper reference for rejecting the recited limitation or allow the claims.

Claim 1 recites *where a number of bits in the subset corresponds to a periodicity of the serial sequence of scramble bits.* Claims 8, 13, and 17 include similar language. Nothing in Lee suggests that the number of parallel bits generated by its generating block 72 has any relation to a periodicity of the input sequence of scramble bits.

[3] Lee, column 6, lines 17-21.
[4] Lee, column 6, lines 66-68 to column 7, lines 1-2.

**Conclusion**

The applicants request reconsideration and allowance of all remaining claims. The applicants encourage examiner to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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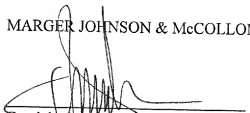

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